ENCAPSULATED METAL STRUCTURES FOR SEMICONDUCTOR DEVICES AND MIM CAPACITORS INCLUDING THE SAME

ABSTRACT OF THE DISCLOSURE

A method is described for fabricating an encapsulated metal structure in a feature formed in a substrate. The sidewalls and bottom of the feature are covered by a barrier layer and the feature is filled with metal, preferably by electroplating. A recess is formed in the metal, and an additional barrier layer is deposited, covering the top surface of the metal and contacting the first barrier layer. The additional barrier layer is planarized, preferably by chemical-mechanical polishing. The method may be used in fabricating a MIM capacitor, with the encapsulated metal structure serving as the lower plate of the capacitor. A second substrate layer is deposited on the top surface of the substrate, with an opening overlying the encapsulated metal structure. A dielectric layer is deposited in the opening, covering the encapsulated metal structure at the bottom thereof. An additional layer, serving as the upper plate of the capacitor, is deposited to cover the dielectric layer and to fill the opening. The dielectric layer and the additional layer are planarized, preferably by CMP.